# PATENT ABSTRACTS OF JAPAN

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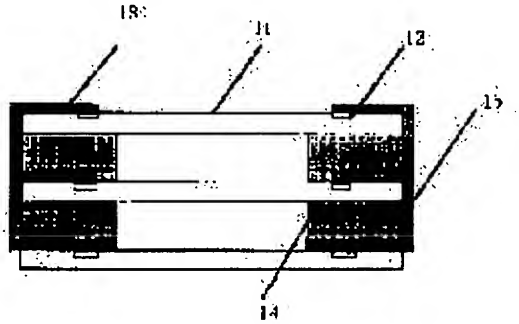
## (54) STACKED SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:

PROBLEM TO BE SOLVED: To easily manufacture chip-on-chip structure where multiple IC are stacked by forming an electric continuity wiring from bonding pads to the end faces of chips, bonding and stacking the chips by means of adhesion resin layers and connecting all the chips stacked by an electric continuity wiring.

SOLUTION: An electric continuity wiring 13 is formed by discharging a molten solder material from an ink jet head from respective bonding pads 12 to a cut part where wiring connection with the other IC chip 11 is assumed. Electron beam curing-type adhesion 14 is applied on the surface of a silicon wafer. The silicon wafer is cut and divided into each IC chip 11. IC having the electric functions of different types are similarly worked and overlapped. Electron beams are radiated and the IC chips 11 are bonded. Then, a continuity wiring 15 is formed by discharging a molten solder material from the ink jet head to the side part of an IC chip stack body where the IC chips 11 are overlapped.

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* NOTICES *



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CLAIMS

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[Claim(s)]
[Claim 1] The laminating mold semiconductor device carry out that all the chips to which the laminating of two or more chips [ have / electrically / another function ] which electric flow wiring was formed by the chip end face from each bonding pad of IC chip, and the existing adhesive resin layer was formed in the whole surface or some of this chip, and were further formed in it similarly was carried out by this resin layer with adhesion and electric flow wiring which a laminating is carried out and come to cross each chip end face further were connected as the description.
[Claim 2] The first process which forms electric flow wiring even in each chip cutting location at least from the bonding pad in each chip of the silicon wafer with which two or more IC chips were formed, The second process which forms the resin layer which has an adhesive property in the whole surface or some of silicon wafer of an electric flow wiring forming face which passed through the first process, The third process which divides into each IC chip the wafer which passed through the second process by cutting, The fourth process which the laminating of the IC chip which was formed similarly, and which has another function electrically is carried out, and is mutually made adhesion by hardening of resin with an adhesive property, The manufacture approach of the laminating mold semiconductor device characterized by consisting of the fifth process at which each IC chip by which the laminating was carried out is connected in the direction which crosses each IC chip cutting plane at the ends of electric flow wiring produced at the first process by electric flow wiring.
[Claim 3] The manufacture approach of the laminating mold semiconductor device according to claim 2 characterized by forming electric flow wiring by the ink jet method.
[Claim 4] The manufacture approach of the laminating mold semiconductor device according to claim 2 characterized by coming to choose an electric flow wiring material out of the conductive resin containing a metal or a conductive particle.
[Claim 5] The manufacture approach of the laminating mold semiconductor device according to claim 2 characterized by being collectively carried out after being carried out whenever hardening of the adhesion resin of IC chip of the fourth process repeats the chip of one sheet, or repeating all IC chips.
[Claim 6] The manufacture approach of the laminating mold semiconductor device according to claim 2 characterized by performing hardening of adhesion resin by heat curing or electron ray hardening.
[Claim 7] The manufacture approach of the laminating mold semiconductor device according to claim 2 characterized by performing the second process which forms a resin layer with an adhesive property after cutting to IC chip of the third process.
[Claim 8] The manufacture approach of the laminating mold semiconductor device according to claim 2 characterized by carrying out after the third process cut to IC chip performs hardening of a laminating and adhesion resin in the state of a silicon wafer.

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the laminating mold IC chip which laminates a semiconductor IC chip and is formed, and its manufacture approach.
[0002]
[Description of the Prior Art] Before, in order to realize structure where packaging density is high, the chip structure on chip which carries out the laminating of the IC chip is proposed, and various proposals are made also to the electrical installation during IC chip in that case. For example, in JP,8-264712,A, as shown in drawing 5 , the gestalt to which IC chip by which the laminating was carried out in the penetrated through hole 52 which was formed in the IC chip 51 is electrically connected by the metal 53 is proposed, and the same is said of JP,5-63137,A. Furthermore by the patent number No. 2605968, the gestalt as which the physical relationship of a bonding pad with the same attribute was also considered is taken.
[0003]
[Problem(s) to be Solved by the Invention] However, in the point which forms the through hole penetrated to IC chip or the silicon wafer with which the integrated circuit was formed by each by the conventional approach, it is not easy. Namely, as for producing a through hole, difficulty follows, without giving a damage to the formed integrated circuit in any way. On the other hand, if a through hole is beforehand formed in the silicon wafer before integrated-circuit formation, causing difficulty to formation of an integrated circuit will be predicted easily.
[0004]
[Means for Solving the Problem] Are for solving the trouble of the above-mentioned conventional technique, and, as for a laminating mold semiconductor device according to claim 1, electric flow wiring is formed by the chip end face from each bonding pad of IC chip. The resin layer which furthermore has an adhesive property in this the whole surface or some of chip is formed. It is characterized by connecting all the chips to which the laminating of two or more chips which were formed similarly, and which have another function electrically was carried out by this resin layer with adhesion and electric flow wiring which a laminating is carried out and comes to cross each chip end face further.
[0005] The first process at which the manufacture approach of a laminating mold semiconductor device according to claim 2 forms electric flow wiring even in each chip cutting location at least from the bonding pad in each chip of the silicon wafer with which two or more IC chips were formed, The second process which forms the resin layer which has an adhesive property in the whole surface or some of silicon wafer of an electric flow wiring forming face which passed through the first process, The third process which divides into each IC chip the wafer which passed through the second process by cutting, The fourth process which the laminating of the IC chip which was formed similarly, and which has another function electrically is carried out, and is mutually made adhesion by hardening of resin with an adhesive property, It is characterized by consisting of the fifth process at which each IC chip by which the laminating was carried out is connected in the direction which crosses each IC chip end face by the end faces of electric flow wiring produced at the first process by electric flow wiring.
[0006] The manufacture approach of a laminating mold semiconductor device according to claim 3 is characterized by forming electric flow wiring by the ink jet method in claim 2.
[0007] It is characterized by coming to choose the manufacture approach of a laminating mold semiconductor device according to claim 4 out of the conductive resin with which an electric flow wiring material contains a metal or a conductive particle in claim 2.
[0008] It is characterized by putting it in block and performing it, after the manufacture approach of a laminating mold semiconductor device according to claim 5 is performed whenever hardening of the adhesion resin of IC chip of the

fourth process repeats the chip of one sheet in claim 2, or it repeats all IC chips.
[0009] The manufacture approach of a laminating mold semiconductor device according to claim 6 is characterized by performing hardening of adhesion resin by heat curing or electron ray hardening in claim 2.
[0010] The manufacture approach of a laminating mold semiconductor device according to claim 7 is characterized by performing the second process which forms the resin layer which has an adhesive property in claim 2, after cutting to IC chip of the third process.
[0011] It is characterized by enforcing the manufacture approach of a laminating mold semiconductor device according to claim 8, after the third process cut to IC chip in claim 2 performs hardening of a laminating and adhesion resin in the state of a silicon wafer.
[0012] (Operation) Explanation is added about formation of electric flow wiring by the ink jet method. Conventionally, the metal membrane was formed by plating or the spatter, and it was further processed into wiring using photolithography, etching, etc. An ink jet method is the ink regurgitation technique of the printer which is the peripheral device of a personal computer originally, and is a technique which breathes out the very small drop beyond about 10 pico l. from a very small nozzle tip, and draws. It has checked that the regurgitation of the metal which the low melting point fused, the metal paste, etc. could be carried out from a head nozzle in recent years. Therefore, the drawing formation of the electric wiring can be directly carried out with this technique. Detailed wiring of a minimum of about 20 micrometers is possible also for wiring width of face. Therefore, this technique has high possibilities as a very easy wiring formation technique in which a large-scale process is not used.
[0013]
[Embodiment of the Invention] An example explains the gestalt of operation of this invention below.
[0014] (Example 1) Drawing 2 shows the silicon wafer of the diameter of 6 inch in which IC chip was formed. Drawing 3 shows a part of the front face, and 31 is a bonding pad for wiring connection. Parts 32 other than a bonding pad are covered by the insulator layer formed by plasma CVD. In this example, what formed the bonding pad only in the periphery of each IC chip was used. Although set to hundreds from dozens, in order to give explanation easy, the number of a bonding pad lessened the number and drew it. Moreover, the continuous-line section 33 shows the location cut at a back process. Each bonding pad is usually formed with aluminum, and is covered in a barrier metal layer if needed. In this example, the titanium tungsten alloy (TiW) and the thing which covered a it top with copper were used.
[0015] The electric flow wiring 34 with a thickness [ of about 10 micrometers ] and a width of face of 30 micrometers was formed by carrying out the regurgitation of the solder ingredient fused from the ink jet head before the cutting section the wiring connection with other IC chips is assumed to be at a back process from each bonding pad as the first process. The metal which can **** in an ink jet has level which can apply the metal fused at 50 to several 100 degrees C in the present condition. In order to raise the adhesion of wiring formed of this, dry type surface treatment, such as plasma etching, may be performed to the silicon wafer with which IC was formed. In this example, light etching of the insulator layer front face on a silicon wafer was carried out by the oxygen plasma.
[0016] The adhesive resin of an electron ray hardening mold was applied to the front face of this silicon wafer as the second process. This adhesive resin was applied to IC chip periphery like 41 of drawing 4 . A resin layer is formed at least after the above-mentioned electric flow wiring. Especially limitation set it to 100 micrometers by this example, although it was thin. An adhesive resin layer is not formed throughout a periphery for the heat generated from IC making it easy to escape outside.
[0017] The silicon wafer produced at all processes as the third process was cut and divided into each IC chip.
[0018] IC which has an electric function of a different kind as the fourth process was processed similarly, and a total of three sheets were piled up. IC chip put on the topmost part did not cover adhesive resin, but the bump by the solder for connecting with the circuit board electrically was formed in each bonding pad. Then, the electron ray was irradiated and IC chip of three sheets was pasted up.
[0019] The electric flow wiring 15 with a thickness [ of about 10 micrometers ] and a width of face of 30 micrometers was formed by carrying out the regurgitation of the solder ingredient which fused the IC chip 11 from the ink jet head in the lateral portion of IC chip layered product piled up three sheets as shown in drawing 1 as the fifth process. Electric flow wiring which formed 12 with the bonding pad and formed 13 at the first process, and 14 are adhesive resin layers. Dry type surface treatment, such as plasma etching, may be performed for the front face of the wiring formation section at least before this wiring formation for washing and a wiring adhesion improvement. In this example, light etching was carried out by the oxygen plasma. This wiring made three-dimensions-electrical installation possible by being joined to the end face of electric flow wiring pulled out from the above-mentioned bonding pad. The high chip structure of packaging density on chip was realizable as mentioned above.
[0020] (Example 2) Although it was the same as that of an example 1, the resin which contained the silver granule child

in the change of electric flow wiring by the metal, and the so-called silver paste were used. Since resistance generally becomes high rather than a metal, they are the thickness of about 30 micrometers, and width of face of 30 micrometers. It formed as wiring. Moreover, the adhesion resin used at the second process used the thermosetting acrylic. Since the silver paste was also a heat-curing mold, package hardening was able to be carried out. The high chip structure of packaging density on chip as well as an example 1 was realizable the above result. Especially if paste material does not affect wiring resistance, it will not be restricted. It is not restricted if the resin and the organic solvent component to contain do not affect other structures, either. The big predominance of this invention is in the ease of a wiring formation process as mentioned above.

[0021] (Example 3) Although it was fundamentally [ as an example 1 ] the same, after performing cutting to each IC chip of the third process immediately after the first process and dividing after washing spreading of the adhesion resin which is originally the second process to each IC chip, it carried out. Since an adhesion resin top was polluted with the dust generated at the time of cutting and washing may also have been hard to remove when it cuts after adhesion resin spreading, it carried out. The high chip structure of packaging density on chip as well as an example 1 was realizable the above result.

[0022] (Example 4) Although it was fundamentally [ as an example 1 ] the same, cutting to each IC chip of the third process was carried out after the second process and the fourth process. That is, after applying adhesion resin on a silicon wafer at the second process, the fourth laminating and a hardening process were performed with the wafer condition. Whenever it repeated a laminating and one hardening, they were carried out according to the heat-curing process. It bundled up in the state of the laminating, and cut. A predominance is in this point that can be cut collectively. The high chip structure of packaging density on chip as well as an example 1 was realizable the above result.

[0023] (Example 5) Although it was the same as that of an example 4, the laminating of a silicon wafer was performed by five sheets, and the electron ray performed hardening at once. Furthermore, it bundled up in the state of the laminating, and cut. The high chip structure of packaging density on chip as well as an example 1 was realizable the above result.

[0024] Although only the ink jet technique is applied as a method of forming electric flow wiring in this example, how to breathe out a metaled minute particle from a detailed nozzle, for example in a vacuum, and form a metal membrane is also examined, and applicability is high also to this invention.

[0025]

[Effect of the Invention] It became possible to manufacture easily the chip structure on chip where the laminating of many ICs was carried out by this invention as mentioned above.

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DRAWINGS

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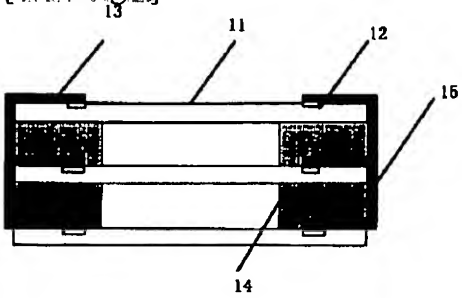
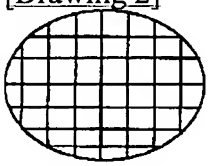
[Drawing 1]




[Drawing 2]



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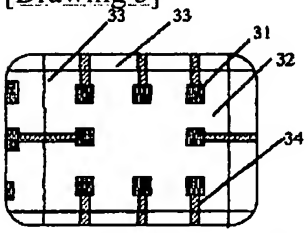


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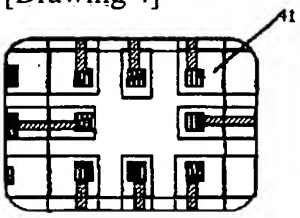
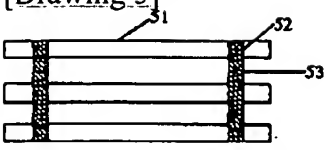



[Drawing 5]

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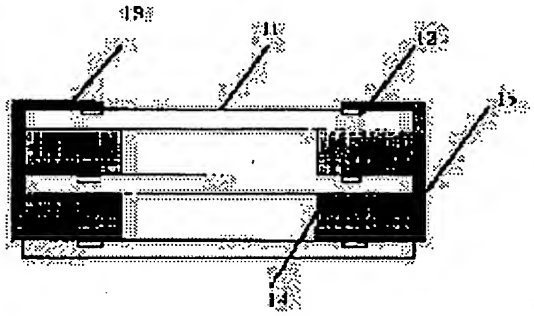


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| 23/52 | | | | |

審査請求　未請求　請求項の数８　ＯＬ　（全　４　頁）

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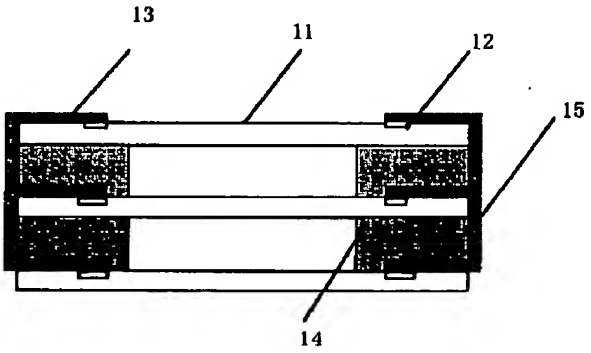
(54)【発明の名称】　積層型半導体装置およびその製造方法

(57)【要約】
【課題】ＩＣを三次元に積層してなるチップオンチップ構造を容易に製造する。
【解決手段】ボンディングパッドからＩＣチップ端面までインクジェット方式により電気的導通配線形成した後、ＩＣチップを接着性樹脂の介在により積層、接着し再度インクジェット方式により電気的導通配線を形成して各ＩＣチップを電気的に接続する。



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【特許請求の範囲】

【請求項１】ＩＣチップの各ボンディングパッドからチップ端面までに電気的導通配線が形成され、さらに該チップの全面もしくは一部に接着性のある樹脂層が形成され、同様に形成された電気的に別機能を持つ複数のチップが該樹脂層により接着、積層され、さらに各チップ端面を横断してなる電気的導通配線により積層された全チップが接続されたことを特徴とする積層型半導体装置。

【請求項２】複数のＩＣチップが形成されたシリコンウエハーの各チップ内のボンディングパッドから少なくとも各チップ切断位置までに電気的導通配線を形成する第一の工程、第一の工程を経たシリコンウエハーの電気的導通配線形成面の全面もしくは一部に接着性のある樹脂層を形成する第二の工程、第二の工程を経たウエハーを切断により個々のＩＣチップに分割する第三の工程、同様に形成された電気的に別機能を持つＩＣチップが積層され、接着性のある樹脂の硬化によって互いに接着にされる第四の工程、積層された各ＩＣチップが第一の工程で作製された電気的導通配線の末端同士で各ＩＣチップ切断面を横断する方向に電気的導通配線により接続される第五の工程からなることを特徴とする積層型半導体装置の製造方法。

【請求項３】電気的導通配線がインクジェット方式で形成されることを特徴とする請求項２記載の積層型半導体装置の製造方法。

【請求項４】電気的導通配線材料が金属もしくは導電性粒子を含有する導電性樹脂から選ばれてなることを特徴とする請求項２記載の積層型半導体装置の製造方法。

【請求項５】第四の工程のＩＣチップの接着樹脂の硬化が一枚のチップを重ねる毎に行われるかもしくは全ＩＣチップを重ねた後に一括して行われることを特徴とする請求項２記載の積層型半導体装置の製造方法。

【請求項６】接着樹脂の硬化が熱硬化もしくは電子線硬化でおこなわれることを特徴とする請求項２記載の積層型半導体装置の製造方法。

【請求項７】接着性のある樹脂層を形成する第二の工程が第三の工程のＩＣチップへの切断の後に行われることを特徴とする請求項２記載の積層型半導体装置の製造方法。

【請求項８】ＩＣチップへ切断する第三の工程がシリコンウエハー状態で積層、接着樹脂の硬化を行った後に実施されることを特徴とする請求項２記載の積層型半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は半導体ＩＣチップを積層化して形成される積層型ＩＣチップおよびその製造方法に関する。

【０００２】

【従来の技術】従来より、実装密度の高い構造を実現するためにＩＣチップを積層するチップオンチップ構造が提案されており、その際ＩＣチップ間の電気的接続にも様々な提案がされている。例えば特開平８－２６４７１２では図５に示されるようにＩＣチップ５１に形成された貫通したスルーホール５２により積層されたＩＣチップが金属５３により電気的に接続される形態が提案されており、また特開平５－６３１３７も同様である。さらには特許番号第２６０５９６８号では同一属性のあるボンディングパッドの位置関係も考慮された形態がとられている。

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【０００３】

【発明が解決しようとする課題】しかしながら従来の方法ではいずれも集積回路の形成されたＩＣチップもしくはシリコンウエハーに貫通したスルーホールを形成する点において容易ではない。すなわち、形成された集積回路に何らダメージを与えることなくスルーホールを作製することは困難が伴う。一方集積回路形成前のシリコンウエハーにあらかじめスルーホールを形成するなら集積回路の形成に困難をきたすことが容易に予測される。

【０００４】

【課題を解決するための手段】上記の従来技術の問題点を解決するためのもので請求項１記載の積層型半導体装置はＩＣチップの各ボンディングパッドからチップ端面までに電気的導通配線が形成され、さらに該チップの全面もしくは一部に接着性のある樹脂層が形成され、同様に形成された電気的に別機能を持つ複数のチップが該樹脂層により接着、積層され、さらに各チップ端面を横断してなる電気的導通配線により積層された全チップが接続されたことを特徴とする。

【０００５】請求項２記載の積層型半導体装置の製造方法は複数のＩＣチップが形成されたシリコンウエハーの各チップ内のボンディングパッドから少なくとも各チップ切断位置までに電気的導通配線を形成する第一の工程、第一の工程を経たシリコンウエハーの電気的導通配線形成面の全面もしくは一部に接着性のある樹脂層を形成する第二の工程、第二の工程を経たウエハーを切断により個々のＩＣチップに分割する第三の工程、同様に形成された電気的に別機能を持つＩＣチップが積層され、接着性のある樹脂の硬化によって互いに接着にされる第四の工程、積層された各ＩＣチップが第一の工程で作製された電気的導通配線の端面同士で各ＩＣチップ端面を横断する方向に電気的導通配線により接続される第五の工程からなることを特徴とする。

【０００６】請求項３記載の積層型半導体装置の製造方法は請求項２において電気的導通配線がインクジェット方式で形成されることを特徴とする。

【０００７】請求項４記載の積層型半導体装置の製造方法は請求項２において電気的導通配線材料が金属もしくは導電性粒子を含有する導電性樹脂から選ばれてなることを特徴とする。

【０００８】請求項５記載の積層型半導体装置の製造方法は請求項２において第四の工程のＩＣチップの接着樹脂の硬化が一枚のチップを重ねる毎に行われるかもしくは全ＩＣチップを重ねた後に一括して行われることを特徴とする。

【０００９】請求項６記載の積層型半導体装置の製造方法は請求項２において接着樹脂の硬化が熱硬化もしくは電子線硬化でおこなわれることを特徴とする。

【００１０】請求項７記載の積層型半導体装置の製造方法は請求項２において接着性のある樹脂層を形成する第二の工程が第三の工程のＩＣチップへの切断の後に行われることを特徴とする。

【００１１】請求項8記載の積層型半導体装置の製造方法は請求項２においてＩＣチップへ切断する第三の工程がシリコンウエハー状態で積層、接着樹脂の硬化を行った後に実施されることを特徴とする。

【００１２】（作用）インクジェット方式による電気的導通配線の形成について説明を加える。従来はメッキあるいはスパッタにより金属膜を形成し、さらにフォトリソグラフィー、エッチング等を用いて配線に加工していた。インクジェット方式とは元来パーソナルコンピュータの周辺機器であるプリンターのインク吐出技術であり１０ピコリットル程度以上の微少液滴を微少ノズル先端から吐出して描画する技術である。近年低融点の溶融した金属、金属ペースト等もヘッドノズルから吐出できることが確認できた。したがってこの技術で直接的に電気的配線が描画形成できる。配線幅も最小２０μm程度の微細配線が可能である。したがって、本技術は大掛かりなプロセスを用いない極めて簡単な配線形成技術として将来性が高い。

【００１３】

【発明の実施の形態】以下本発明の実施の形態を実施例により説明する。

【００１４】（実施例１）図２はＩＣチップを形成した６インチ径のシリコンウエハーを示す。図３はその表面の一部を示すもので３１は配線接続用のボンディングパッドである。ボンディングパッド以外の部分３２はプラズマＣＶＤで形成した絶縁膜で覆われている。本実施例では各ＩＣチップの周辺部のみにボンディングパッドを形成したものを用いた。ボンディングパッドの個数は数十から数百になるが説明を容易にするために個数を少なくして描いた。また実線部３３は後工程で切断される位置を示す。各ボンディングパッドは通常アルミニウムで形成されており必要に応じてバリアメタル層でカバーされる。本実施例ではチタンタングステン合金（ＴｉＷ）とその上を銅でカバーしたものを用いた。

【００１５】第一の工程として各ボンディングパッドから後工程で他のＩＣチップとの配線接続が想定される切断部までの間にインクジェットヘッドから溶融したはんだ材料を吐出することにより厚み約１０μm、幅３０μm



の電気的導通配線３４を形成した。インクジェットで塗出できる金属は現状では５０℃から数１００℃で溶融する金属が適用できるレベルになってきた。これによって形成される配線の密着性を高めるためにＩＣが形成されたシリコンウエハーにプラズマエッチングなどの乾式表面処理を行ってもよい。本実施例では酸素プラズマによってシリコンウエハーの上の絶縁膜表面をライトエッチングした。

【００１６】第二の工程としてこのシリコンウエハーの表面に電子線硬化型の接着性樹脂を塗布した。該接着性樹脂はＩＣチップ周辺部に図４の４１のように塗布された。少なくとも上記電気的導通配線の上には樹脂層が形成される。厚みは特に限定はないが本実施例では１００μmとした。周辺部全域に接着性樹脂層を形成しないのはＩＣから発生する熱が外部に逃げ易くするためである。

【００１７】第三の工程として全工程で作製したシリコンウエハーを一つ一つのＩＣチップに切断して分割した。

【００１８】第四の工程として異種の電気的機能を持つＩＣを同様に加工して計３枚を重ねあわせた。最上部に置かれたＩＣチップは接着性樹脂を被覆せず各ボンディングパッドには回路基板に電気的に接続するためのはんだによるバンプが形成された。続いて電子線を照射して三枚のＩＣチップを接着した。

【００１９】第五の工程として図１に示すようにＩＣチップ１１を三枚重ね合せたＩＣチップ積層体の側面部においてインクジェットヘッドから溶融したはんだ材料を吐出することにより厚み約１０μm、幅３０μmの電気的導通配線１５を形成した。１２はボンディングパッド、１３は第一の工程で形成した電気的導通配線、１４は接着性樹脂層である。この配線形成前に少なくとも配線形成部の表面を洗浄と配線密着性改善のためプラズマエッチングなどの乾式表面処理を行ってもよい。本実施例では酸素プラズマによってライトエッチングした。この配線は前述のボンディングパッドから引き出した電気的導通配線の端面と接合されることにより三次元的な電気的接続を可能にした。以上のようにして実装密度の高いチップオンチップ構造が実現できた。

【００２０】（実施例２）実施例１と同様であるが金属による電気的導通配線の変わりに銀粒子を含んだ樹脂、所謂銀ペーストを用いた。一般に金属よりは抵抗が高くなるため厚み約３０μm、幅３０μm の配線として形成した。また第二の工程で用いる接着樹脂は熱硬化性アクリルを用いた。銀ペーストも熱硬化型であったため一括硬化できた。以上の結果実施例１と同様に実装密度の高いチップオンチップ構造が実現できた。ペースト材は配線抵抗に影響を与えないなら特に制限されない。含有する樹脂、有機溶剤成分も他の構造に影響を与えなければ制限されない。以上のように本発明の大きな優位性は配線

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形成工程の容易性にある。

【００２１】（実施例３）実施例１と基本的には同様であるが第三の工程の個々のＩＣチップへの切断を第一の工程の直後に行い、洗浄の後本来第二の工程である接着樹脂の塗布を各ＩＣチップへ分割してから実施した。接着樹脂塗布後に切断すると接着樹脂上が切断時に発生する粉塵で汚染され洗浄によっても除去しにくいことがあるため実施した。以上の結果実施例１と同様に実装密度の高いチップオンチップ構造が実現できた。

【００２２】（実施例４）実施例１と基本的には同様であるが第三の工程の個々のＩＣチップへの切断を第二の工程と第四の工程の後に実施した。すなわち、第二の工程でシリコンウエハー上に接着樹脂を塗布した後第四の積層、硬化工程をウエハー状態のまま行った。積層、硬化は一枚重ねるごとに熱硬化工程により実施した。積層状態で一括して切断した。この一括して切断できる点に優位性がある。以上の結果実施例１と同様に実装密度の高いチップオンチップ構造が実現できた。

【００２３】（実施例５）実施例４と同様であるがシリコンウエハーの積層を５枚で行い、硬化は電子線により一回で行った。さらに積層状態で一括して切断した。以上の結果実施例１と同様に実装密度の高いチップオンチップ構造が実現できた。

【００２４】本実施例では電気的導通配線の形成法としてインクジェット技術のみを適用しているが、例えば真空中で微細ノズルから金属の微小粒子を吐出して金属膜を形成する方法も検討されており本発明に対しても適用

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可能性が高い。

【００２５】

【発明の効果】以上のように本発明により多数のＩＣが積層されたチップオンチップ構造を容易に製造することが可能となった。

【図面の簡単な説明】

【図１】本発明の一つの実施例を模式的に示す断面図。

【図２】本発明で用いたＩＣチップが形成されたシリコンウエハーを模式的に示す図。

【図３】実施例１の第一の工程を説明するための図。

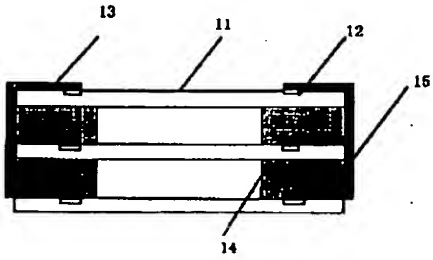
【図４】実施例１の第二の工程を説明するための図。

【図５】従来の一例を示す図。

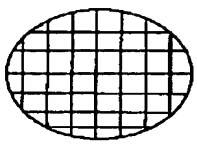
【符号の説明】

１１．ＩＣチップ
１２．ボンディングパッド
１３．電気的導通配線
１４．接着性樹脂
１５．電気的導通配線
３１．ボンディングパッド
３２．絶縁膜で被覆された部分
３３．切断位置
３４．電気的導通配線
４１．接着性樹脂塗布部
５１．ＩＣチップ
５２．スルーホール
５３．金属配線

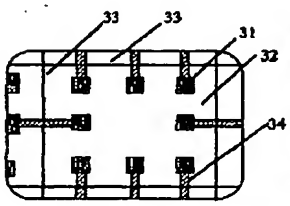
【図１】



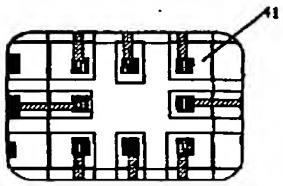

【図２】



【図３】




【図４】




【図５】